

# Design and simulation of high-swing fully differential telescopic Op-Amp

**Zahra Pezeshki**

Faculty of Electrical and Robotic Engineering, Shahrood University of Technology, Shahrood, Semnan, Iran

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## ABSTRACT

This article describes the process of design and simulation of a high-swing fully differential telescopic operational amplifier (Op-Amp). Due to the common gate-common source (CG and CS) cascode structure, the gain is very high. To maximize this gain, the load must also be selected such as two current sources. This circuit has the higher voltage in output than current Op-Amps in accordance with desirable characteristics. The loss of power of this operating amplifier are very low and in milliwatts. With use of a power supply of 1.8 V, it achieves a high-swing 1.2 V, a differential gain of 76.333 dB,  $\omega_{uGB}$  of 412 MHz, and >50 dB CMRR. This new design through the simulations and analytically shows that the high-swing fully differential telescopic Op-Amp retains its high CMRR even at high frequencies.

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## Corresponding Author:

Zahra Pezeshki

Faculty of Electrical and Robotic Engineering

Shahrood University of Technology

Shahrood, Semnan, Iran

Email: tejaratemrooz@gmail.com

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## 1. INTRODUCTION

The simplest operational amplifier (Op-Amp) is a high-gain differential amplifier. The amount of this gain in the range of  $10^1$ - $10^5$  is sufficient for Op-Amp applications. Op-Amp performance parameters are: open-loop gain, small signal bandwidth, large signal bandwidth, output swing, linearity, noise, offset and supply rejection [1], [2]. By designing an Op-Amp, these parameters are communicated with each other. Single cascode differential amplifiers with integrated components can hardly produce much gain. The bandwidth is determined by the load capacitance. To achieve the high gain, differential cascodes are used. These cascode connections lie between power supplies and load current sources. When the MOSFETs of each branch are aligned with each other, they create a telescopic-like structure. Therefore, this type of configuration is known as telescopic Op-Amp. The resulting circuit is symmetric with each of the output loads generated by the cascade current source. Their output swings are also limited due to the short-circuit problem of one of the inputs to the output in the applications such as source follower [3]. Another problem is power consumption. There are various designs that they have tried to reach high swing with low power consumption, but the power consumption value has not been reported [3]. In some papers, output swing is low or has not been reported too [4], [5]. The gain-boosted telescopic Op-amps can reach to high swing with low power consumption, but their design is classified into multiple design:

- folded cascode Op-amp [6].
- the main Op-amp and the boosting Op-amp [7], [8].
- the main Op-amp and the multiplying digital-to-analog converter (MDAC) architecture [9].
- the main Op-amp and the Miller compensation [10].

So, such a design implementation is very complicated. In this paper, author want to design a high-swing fully differential telescopic Op-Amp in 0.18  $\mu\text{m}$  CMOS technology. All simulations of this circuit are performed in HSPICE RF software. Other softwares such as Cadence can also be used in this regard [2].

Figure 1 shows the fully differential telescopic Op-Amp. The fully differential designs include the first and secondly switched current mirrors and the output which can be a circuit duo to boosting the gain and reaching the wide band [11]-[17], but this can cause the power consumption to increase. Biasing also can improve the gain with less dissipation, e.g. wideband QFG dynamic biasing (QFG-DB) Op-amp, but it cannot to increase the output or input voltage [18]. Some applications such as fully differential difference transconductance amplifier (FDDTA), require low output, so the high gain is not important in their design. Because they are utilized as a low pass filter [19]. The advantage of the fully differential design is that the differential mode signal path encompasses only the n-channel MOSFETs [20]. Only NMOS transistors conduct time-varying currents, and PMOS transistors transmit a constant current. This increases the Op-Amp speed, so the mobility of the n-channel MOSFET is greater than that of the p-channel MOSFET. In my design, we use the telescopic Op-Amp [8] of Figure 1. It is a combination of common gate-common source (CS-CG) that achieves higher gain due to double load of current source.

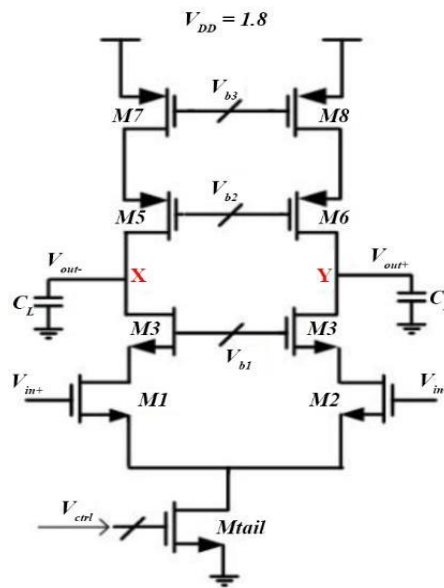


Figure 1. Telescopic cascode with NMOS inputs

Combination of CS-CG cascodes with components such as NMOS is for higher gain. Cascade load current sources with components such as PMOS are used to achieve greater drain resistance, which is used to combine CS-CG cascodes. The gain of the circuit in Figure 1 can be obtained by using half of the circuit as (1) [21].

$$A = g_{mN}[(g_{mN}r_{ON}^2) \parallel (g_{mP}r_{OP}^2)] \quad (1)$$

Where  $g_m$  is the cross-conductivity and  $r_o$  is the drain resistors in the MOSFETs. So, the gain of the telescopic cascode Op-Amp increases. The output swing is as (2):

$$V_{cmo} = 2[V_{DD} - (V_{OD1} + V_{OD3} + V_{ODtail} + |V_{OD5}| + |V_{OD7}|)] \quad (2)$$

Where, the  $V_{OD}$  is overdrive voltage of the MOSFETs, and  $V_{ODtail}$  reduce through the Mtail MOSFET current source,  $I_{total}$ . The output voltage of this circuit is much less than that of a simple fully differential Op-Amp. So, in this paper, I want to design a new fully differential telescopic Op-amp with specifications as shown in Table 1.

Table 1. The characteristic of high-swing fully differential telescopic OP-AMP circuit

Parameter	Characteristic
Gain	> 60 dB
CMRR	> 50 dB
$\omega_{uGB}$	> $2\pi \times 400$ MHz
Phase margin	> 60
Slow Rate	> 200 V/ $\mu$ s
$V_{cmi}$	= 1 V
$V_{cmo}$	= 1.1 V
Output Swing	> 0.5 V
Power Consumption	> = 1.2 mW
Power supply ( $V_{DD}$ )	1.8 V

## 2. THE PROPOSED METHOD

According to the Table 1, author must also consider other features of the telescopic cascade and add to the MOSFETs including  $\mu_n C_{ox} = 200 \frac{\mu A}{V^2}$ ,  $\mu_p C_{ox} = 80 \frac{\mu A}{V^2}$ , body modulation effects:  $\lambda_n = 0.18 V^{-1}$  and  $\lambda_p = 0.36 V^{-1}$ , and the threshold voltage:  $V_{THN} = |V_{THP}| = 0.45 V$  [3], [4]. In this circuit, the total power consumption should not exceed 1.2 mW. The current source of  $V_{DD}$  is  $I_{tail} = 1.2 \frac{mW}{1.80 V} = 0.67 mA$ . So, each cascode branch of the Op-Amp requires 0.34 mA current, means  $I_{tail}/2$ . On the other hand, the common mode output voltage is 1.1 V. That is, each node X and Y in Figure 1 should be able to swing up to 1.1 volt and keep the transistors  $M_3 - M_6$  in saturation area. With a 1.8 V power supply, the total voltage available for  $M_{tail}$  and each cascode branch is 0.7 V. Thus, we have (3):

$$V_{OD1} + V_{OD3} + |V_{OD5}| + |V_{OD7}| + V_{ODtail} = 1.8 - 1.1 = 0.7 \quad (3)$$

Since  $M_{tail}$  draws most of the current, one fifth of the voltage reaches to it, so  $V_{ODtail} = 0.14 V$  and 0.56 V remains for the four cascode transistors. The  $M_5 - M_8$  current sources have low mobility, so more voltage should be allocated per branch to them (0.32 V). Therefore, in a cascode branch, we have  $V_{OD5} + V_{OD7} = 0.32 V$ . The rest of the voltage is allocated to transistors  $M_1$  and  $M_3$ . That is  $V_{OD1} + V_{OD3} = 0.24 V$ . So, the overdrive voltage of transistors 5 and 7 is 0.16 V and the voltage of transistors 1 and 3 is 0.12 V. The aspect ratio of  $M_1 - M_{tail}$  can be evaluated by the bias current and the overdrive voltage of each MOSFET. The relation of drain current to saturation area is (4):

$$I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2 \quad (4)$$

To minimize the parasitic capacitors of the integrated devices, the minimum length of each MOSFET transistor is  $L = 0.18 \mu m$ .

Then,  $(W)_{1-4} = 38 \mu m$ ,  $(W)_{5-8} = 58.25 \mu m$  and  $W_{tail} = 58.775 \mu m$  are obtained. So, the design was done according to the total power consumption, power supply and output swing. The amount of the gain can now be calculated from the (5),

$$A_v \approx g_{m1}[(g_{m3}r_{o3}r_{o1}) \parallel (g_{m5}r_{o5}r_{o7})] \quad (5)$$

By choosing a minimum channel length of  $0.18 \mu m$  for all MOSFET transistors we have  $g_m$  and  $r_o$  which are obtained from (6) and (7).

$$g_m = 2I_D/V_{OD} \quad (6)$$

$$r_o = 1/\lambda I_D \quad (7)$$

So, author have:

$$g_{m1-4} = \frac{2 \times 0.32 \times 10^{-3}}{0.123} = 5.203 \frac{mA}{V}$$

$$g_{m5-8} = \frac{2 \times 0.32 \times 10^{-3}}{0.157} = 4.764 \frac{mA}{V}$$



To keep the all transistors in the saturation area, the bias voltages, control voltage, and maximum and minimum input voltages,  $V_{CMI}$ , are calculated to drive the transistors to the saturation area as:

$$\begin{aligned} V_{ctrl} &= V_{Gstail} \text{ if } V_{ODtail} > V_{Gstail} - V_{th} \\ V_{b1} &= V_{GS3} + V_{ODM1} + V_{ODtail} \text{ if } V_{OD3} > V_{GS3} - V_{th} \\ V_{b2} &= V_{DD} - V_{ODM7} - V_{GS5} \text{ if } V_{OD5} < V_{GS5} - V_{th} \\ V_{b3} &= V_{DD} - V_{GS7} \text{ if } V_{OD7} < V_{GS7} - V_{th} \\ \{V_{inMax} &= V_{DD} - 2V_{OD7} - V_{OD3} \text{ and } V_{inmin} = V_{GS1} + V_{ODtail} \text{ if } V_{OD1} > V_{GS1} - V_{th}\} \end{aligned}$$

So after simulation, all transistors are active and their current are regulated which the total power consumption of the circuit obtains as  $1.2 \text{ mW}$  see Figure 4.

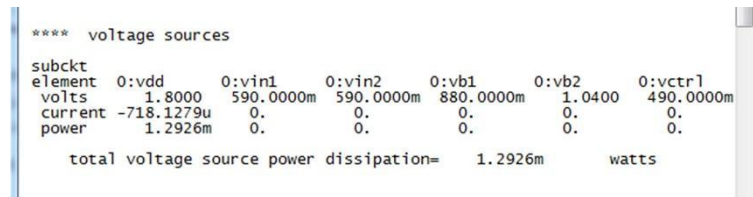


Figure 4. Power consumption of the circuit ( $P_{diss}$ ).

### 3. RESULTS AND DISCUSSION

In this section, author want to discuss about the simulation. According to the Figure 4, the current drawn from the power supply is  $0.72 \text{ mA}$  and the total power consumption of the circuit is  $1.2 \text{ mW}$ . The output voltage response as shown in Figure 5 is  $1.2 \text{ V}$ .

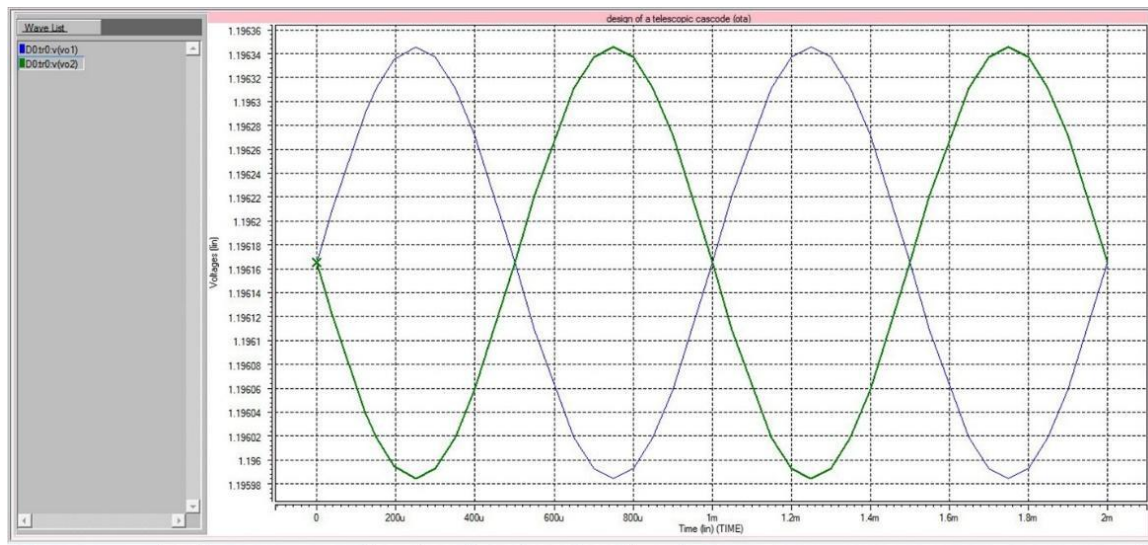


Figure 5. The output swing of the proposed high-swing fully differential telescopic Op-Amp circuit

In Figure 6, the circuit gain is greater than  $60 \text{ dB}$  and  $76.333 \text{ dB}$  ( $111.75 - 35.417 = 76.333 \text{ dB}$ ). So, the Common Mode Rejection Ratio (CMRR) is greater than  $50 \text{ dB}$ .

At frequency of  $412 \text{ MHz}$ , the gain reaches one and thus the unity-gain frequency value,  $\omega_{UGB}$ , is  $412 \text{ MHz}$  see Figure 7.

According to the Figure 7, at the  $\omega_{UGB} = 412 \text{ MHz}$ , the output phase value of the system is  $-61.7^\circ$ , so the phase margin (PM) of the circuit is  $180^\circ - 61.7^\circ = 118.3^\circ$ , which a desirable value is. Further, the total harmonic distortion (THD) of the circuit is  $0.332\%$  for both  $V_{O1}$  and  $V_{O2}$  outputs see Figure 8.

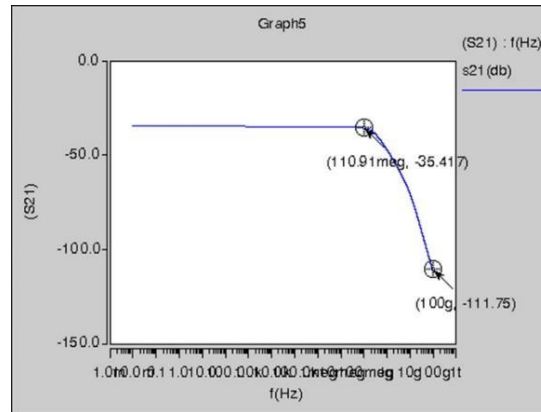


Figure 6. Frequency response of the proposed high-swing fully differential telescopic Op-Amp circuit

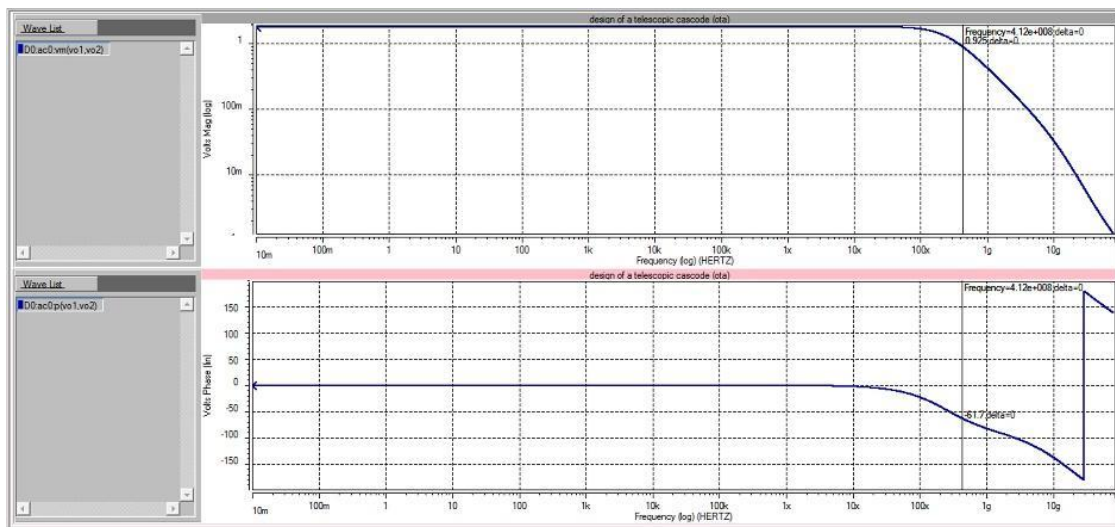


Figure 7. The  $\omega_{UGB}$  and the output system phase of the proposed high-swing fully differential telescopic Op-Amp circuit

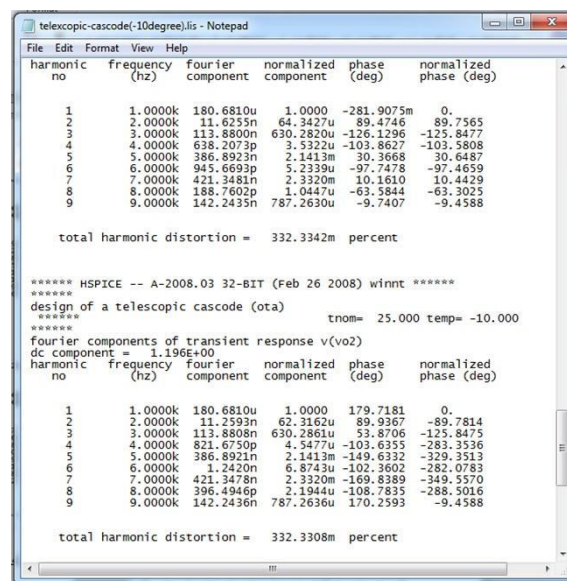


Figure 8. The THD of the proposed high-swing fully differential telescopic Op-Amp circuit

Author can calculate the slow rate as (8) [7], [22].

$$SR \equiv dV_{out}/dt|_{Max} = I_{tail}/C_L = (2I_{DM1.2})/C_L \quad (8)$$

Where  $I_{DM1.2}$  is the bias current of transistors 1 and 2. The value of the slow rate is obtained 261.25 volts per microsecond (MHz) from the simulation see Figure 9.

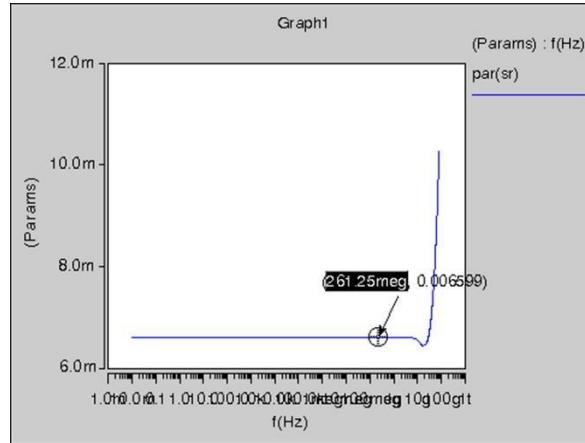


Figure 9. The slow rate of high-swing fully differential telescopic Op-Amp circuit

For noise analysis, I have to send the noise to the system, for example, with a 50 ohmic pull-up resistor (p1): p1 in 0 port=1 ac=0.1 dc=2.1 z0=50

The resistance value from the  $V_{O1}$  output to  $V_{DD}$  is calculated  $g_{m5}r_{o5}r_{o7}$ , which is 359 k $\Omega$ . The output noise is 101.9337 $\mu$ Volts see Figure 10.

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**** the results of the sqrt of integral (v**2 / freq)
      from fstart upto 71.6382g hz. using more freq points
      results in more accurate total noise values.

**** total output noise voltage = 101.9337u volts
**** total equivalent input noise = 0.
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Figure 10. The output noise of the proposed high-swing fully differential telescopic Op-Amp circuit

The characteristic table of the proposed high-swing fully differential telescopic Op-Amp circuit is as Table 2.

Table 2. The Characteristic of the proposed high-swing fully differential telescopic OP-Amp circuit

Characteristic	Description
Power supply	1.8V
Power consumption	1.2 mW
Gain	76.333 dB
$\omega_{UGB}$	412 MHz
Output Phase Value	-61.7°
PM	118.3°
THD	0.332%
Slow Rate	261.25 MHz
Total Output Noise Voltage	101.9337 $\mu$ V
Output Swing Voltage	1.2 V
CMRR	> 50dB

The value of  $(A_v \times \omega_{UGB})/P_{diss}$  obtains as:

$$(A_v \times \omega_{UGB})/P_{diss} = (76.333 \times 412 \times 10^6)/(1.2 \times 10^{-3}) \cong 26207.7 \times 10^9 \text{ dB} \cdot \text{Hz}/\text{Watt}$$

The characteristic of this proposed Op-amp is good comparing the other Op-amps. Table 3 compares the characteristic of this Op-amp with other designs.

Table 3. Comparison the Characteristic of the proposed high-swing fully differential telescopic OP-Amp circuit with other circuits

Characteristic	The proposed Op-amp	QFGD B op-amp [3]	Fully Differential Gain-Boosted Telescopic Cascode Op-amp [7]	Telescopic Op-amp for MDAC [9]	High-Swing CMOS Telescopic Operational Amplifier [8]	Folded - cascode Op-amp [6]	Telescopic Op-Amp with Improved Gain [10]	Dc-Gain Enhanced CMOS Telescopic Op-Amp [5]	Fully-differential Op-amp [15]
Power supply	1.8	< 1	3.3	1.8	3.3	3.3	5	-	1.8
Power consumption (mW)	1.2	-	3.89	0.051	-	9-14	-	5	-
Gain (dB)	76.333	60.5	129	62.81	105	-	85	> 61	> 60
$\omega_{UGB}$ (MHz)	412	65	161	285.6	93	1.3GHz	177.1	1GHz	> 50
Output Phase Value (°)	-61.7	-	-	-	-	-	-	-	-
PM (°)	118.3	81	70.6	57.42	78	-	-	81	60
THD (%)	0.332	-	-	-	-	-	-	-	-
Slow Rate (V/μs)	261.25	-	92	2.19	133	-	-	-	> 100
Total Output Noise Voltage (μV)	101.933	-	-	-	-	-	-	-	-
Output Swing Voltage (V)	7	-	3	-	2.4	-	-	-	> 2.7
CMRR (dB)	>50	>50	>50	-	>50	-	-	-	-

#### 4. CONCLUSION

This paper presents the design of an of high-swing fully differential telescopic Op-Amp circuit with 0.18 CMOS technology. The results of the circuit simulation with HSPICE RF software show that the circuit parameters have acceptable values. One of the important features that this paper wants to acquire is higher voltage than current Op-Amps in accordance with desirable parameters. Finally, by compromising the circuit parameters, we were able to obtain a good performance from the circuit design. As the amplification of signals in many electronic circuits plays a key role and can be easily implemented with Op-Amp, this design can demonstrate this reality which can implemented in a Very Large-Scale Integration (VLSI) chip.

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Zahra Pezeshki is a Master holder in Electronic Integrated Circuits. She's worked on electronic circuit design and project management from 2002 to now as well as obtained one patent in 2007 for solving irrigation problems. Furthermore, she has cooperated with Iran Construction Engineering Organization (IRCEO) as a researcher since 2012 whereas she works on developing new BIM standards for construction industry. Currently, she works as an engineer, senior lecturer and a journalist working with IRCEO and Iranian press. She is greatly interested in energy issues, sustainability and optimization. Her research activities are highly in design, modeling, programming and manufacturing of electrical maps, electrical boards and AI devices to increase thermal comfort and save energy.